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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/751,233 | 12/28/2000 | Ronald E. Gareis | 30GF-1107 | 8771 |

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| EXAMINER | |
|---|---|
| YANCHUS III, PAUL B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/751,233 | GAREIS ET AL. | |
| | Examiner | Art Unit | |
| | Paul B Yanchus | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11,13-16,20 and 22-25* is/are rejected.

7)☒ Claim(s) *7-10,12,17-19,21 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election with traverse of the restriction requirement of claims 1-28 in the reply filed on 7/30/04 is acknowledged. The traversal is on the ground(s) that the subject matter in Groups I and II is related. The Applicant's arguments are found to be persuasive.

The restriction requirement of claims 1-28 is withdrawn.

### *Oath/Declaration*

Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The term "relatively" in claims 3, 13 and 22 is a relative term which renders the claim indefinite. The term " relatively " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danstrom, US Patent no. 5,617,014 and Heaston, Jr. et al., US Patent no. 5,748,422 [Heaston], in view of, Huang et al., US Patent no. 6,133,757 [Huang].

Regarding claim 1, Danstrom teaches implementing a PWM current regulator [switching regulator] including a switching transistor [switching transistor, column 2, line 60 – column 3, line 4]. Danstrom does not specifically teach that the switching transistor is a FET switch. However, as shown by Heaston, using a FET as a switching device is well known in the art [column 6, lines 34-39]. It would have been obvious to one of ordinary skill in the art to use a FET switching device in the Danstrom driving circuit. One would be motivated to use a FET switching device as opposed to another transistor switching device because FET switching devices require less driving current than other transistor switching devices and consequently consume less power and dissipate less heat [Heaston, column 6, lines 40-46].

Danstrom and Heaston do not explicitly teach utilizing the turn on delay of a FET switch to provide a wide operating range of current. Huang teaches that it is well known in the art that the driving current of a FET is directly proportional to the switching speed of the FET [column 7, lines 47-49]. It would have been obvious to one of ordinary skill in the art to use the turn on time of a switching FET to provide a wider operating range of current since it is a well known

concept in the art that the current driving capabilities of a FET are proportional to the switching speed of the FET.

Regarding claim 2, Danstrom teaches implementing a PWM current regulator including a feedback control loop [column 3, lines 20-28].

Regarding claims 4-6, as described above, Huang teaches that it is well known in the art that the driving current of a FET is directly proportional to the switching speed of the FET. Therefore it would have been obvious to one of ordinary skill in the art to adjust the turn on delay of the FET by the proportional amount of time needed to achieve an operating range of current greater than two hundred to one in order to enable the circuit to be compatible with a variety of applications.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, US Patent no. 4,774,450, in view of, Heaston, Jr. et al., US Patent no. 5,748,422 [Heaston].

Kitamura teaches a circuit comprising:

a drive circuit [column 4, line 41 and element 14 in Figure 1];

an output circuit including a load terminal [column 4, lines 41-42 and element 16 in Figure 1];

a feedback amplifier connected to said output circuit [element 40 in Figure 1]; and

an error amplifier circuit connected to said feedback amplifier [column 4, lines 38-41 and element 12 in Figure 1].

Kitamura does not specifically teach that the drive circuit comprises a FET switch. However, as shown by Heaston, using a FET as a switching device is well known in the art

[column 6, lines 34-39]. It would have been obvious to one of ordinary skill in the art to use a FET switching device in the Kitamura driving circuit. One would be motivated to use a FET switching device as opposed to another transistor switching device because FET switching devices require less driving current than other transistor switching devices and consequently consume less power and dissipate less heat [Heaston, column 6, lines 40-46].

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura, US Patent no. 4,774,450 and Heaston, Jr. et al., US Patent no. 5,748,422 [Heaston], in view of, Huang et al., US Patent no. 6,133,757 [Huang].

Danstrom and Heaston, as described above, teach a circuit comprising a drive circuit with a FET, but do not explicitly teach utilizing the turn on delay of the FET switch to provide a wide operating range of current. Huang teaches that it is well known in the art that the driving current of a FET is directly proportional to the switching speed of the FET [column 7, lines 47-49]. It would have been obvious to one of ordinary skill in the art to use the turn on time of a switching FET to provide a wider operating range of current since it is a well known concept in the art that the current driving capabilities of a FET are proportional to the switching speed of the FET.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shamouilian et al., US Patent no. 6,432,282 [Shamouilian], in view of Kitamura, US Patent no. 4,774,450, and Heaston, Jr. et al., US Patent no. 5,748,422 [Heaston].

Kitamura teaches a circuit comprising:

a drive circuit [column 4, line 41 and element 14 in Figure 1];

an output circuit including a load terminal [column 4, lines 41-42 and element 16 in Figure 1];

a feedback amplifier connected to said output circuit [element 40 in Figure 1]; and

an error amplifier circuit connected to said feedback amplifier [column 4, lines 38-41 and element 12 in Figure 1].

Kitamura discloses that the circuit is a voltage regulator, but does not explicitly disclose that the circuit may operate as a current regulator. However, a voltage regulator is essentially a current regulator since current can easily be calculated from voltage. Therefore, Kitamura discloses a circuit, which may operate as a current regulator.

Kitamura does not specifically teach that the drive circuit comprises a FET switch. However, as shown by Heaston, using a FET as a switching device is well known in the art [column 6, lines 34-39]. It would have been obvious to one of ordinary skill in the art to use a FET switching device in the Kitamura driving circuit. One would be motivated to use a FET switching device as opposed to another transistor switching device because FET switching devices require less driving current than other transistor switching devices and consequently consume less power and dissipate less heat [Heaston, column 6, lines 40-46].

Kitamura and Heaston do not disclose including the current regulator in a system comprising a CPU, bus interface, memory and I/O module. However, as shown by Shamouilian, computer systems comprising a CPU, a bus interface, a memory, a I/O module are well known in the art [Figure 2]. It would have been obvious to one of ordinary skill in the art to include the

current regulating circuit taught by Kitamura and Heaston in a well known computer system to ensure that a stable current is supplied to the circuits coupled the computer system.

Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shamouilian et al., US Patent no. 6,432,282 [Shamouilian], Kitamura, US Patent no. 4,774,450, and Heaston, Jr. et al., US Patent no. 5,748,422 [Heaston], in view of, Huang et al., US Patent no. 6,133,757 [Huang].

Shamouilian, Kitamura and Heaston, as described above, teach a circuit comprising a current regulator drive circuit with a FET, but do not explicitly teach utilizing the turn on delay of the FET switch to provide a wide operating range of current. Huang teaches that it is well known in the art that the driving current of a FET is directly proportional to the switching speed of the FET [column 7, lines 47-49]. It would have been obvious to one of ordinary skill in the art to use the turn on time of a switching FET to provide a wider operating range of current since it is a well known concept in the art that the current driving capabilities of a FET are proportional to the switching speed of the FET.

### *Allowable Subject Matter*

Claims 7-10, 12, 17-19, 21 and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hausman, Jr. et al., US Patent no. 6,347,028 teaches a device with a FET drive circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
October 26, 2004

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